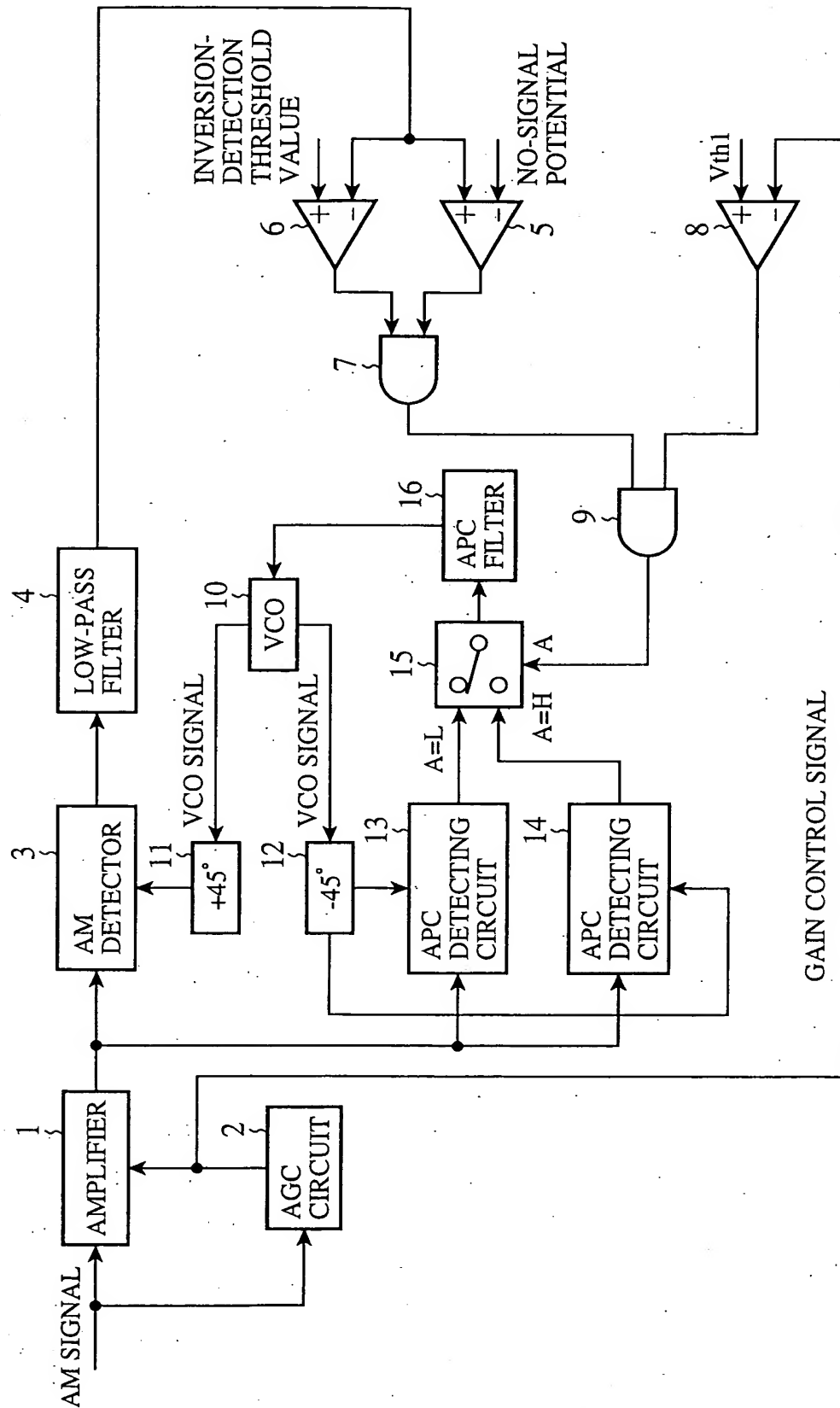


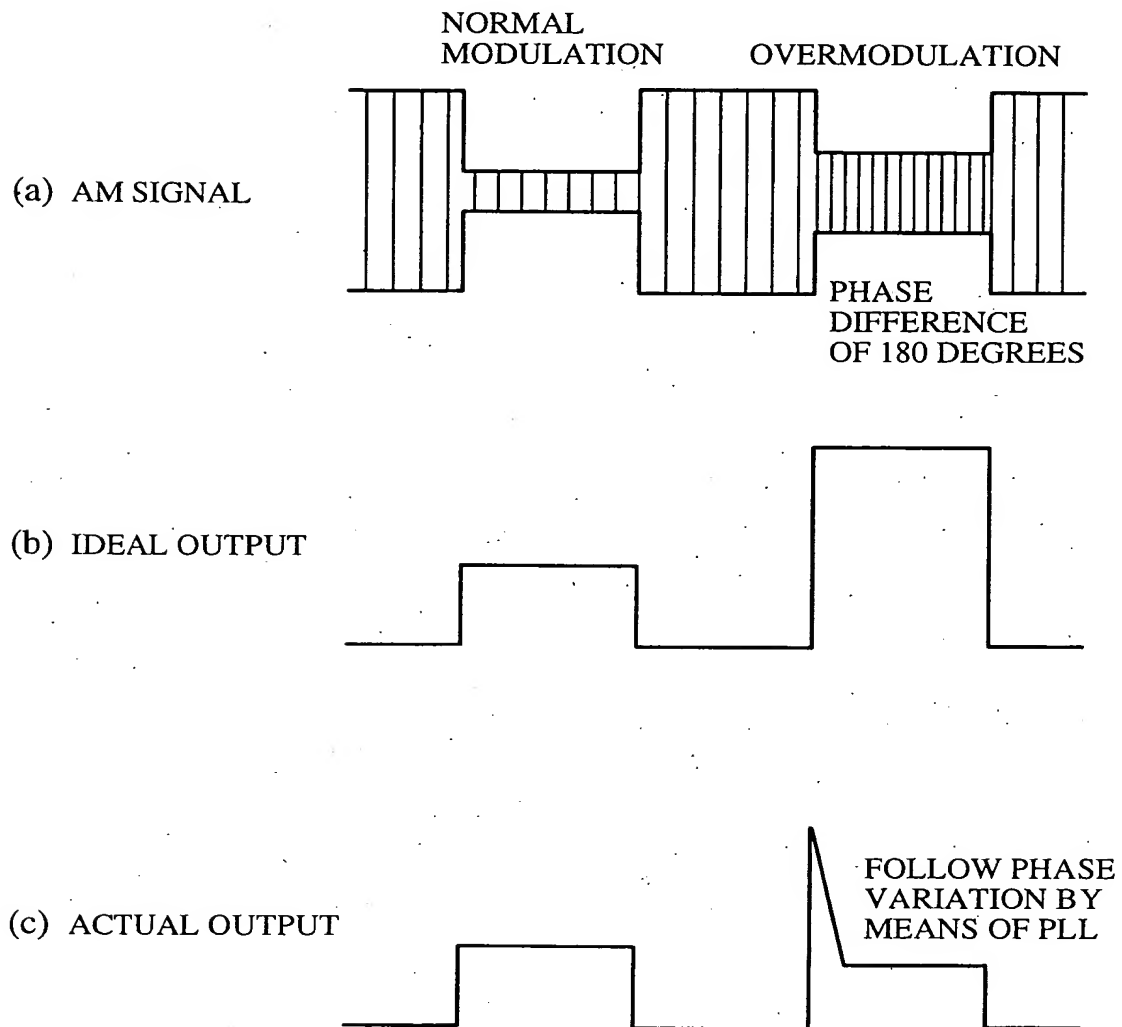
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FIG.1



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FIG.2



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FIG.3

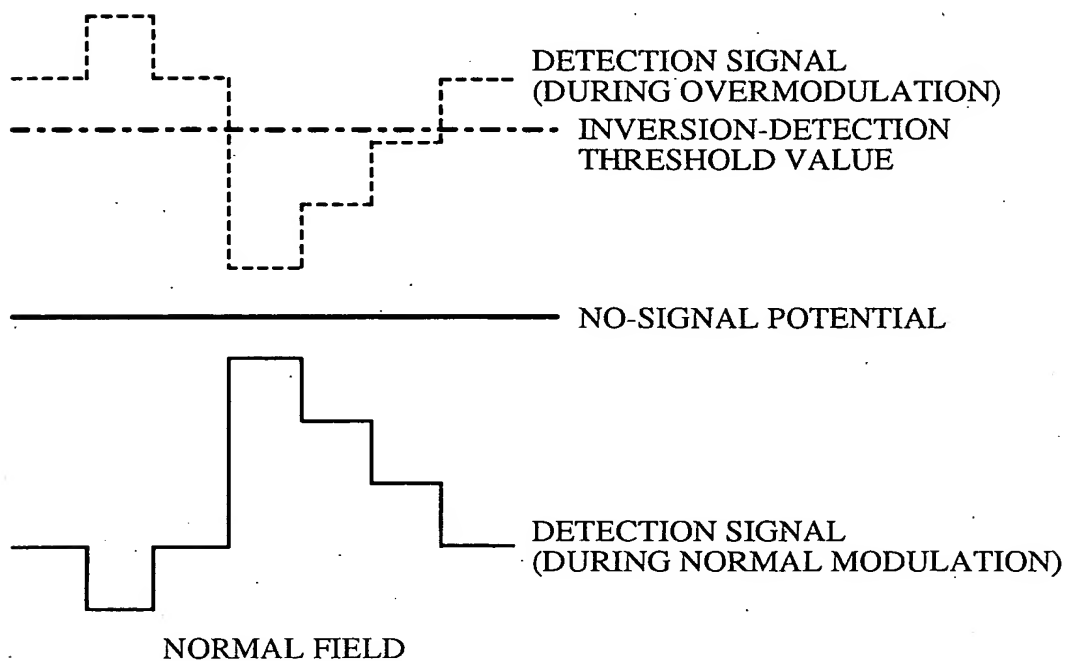
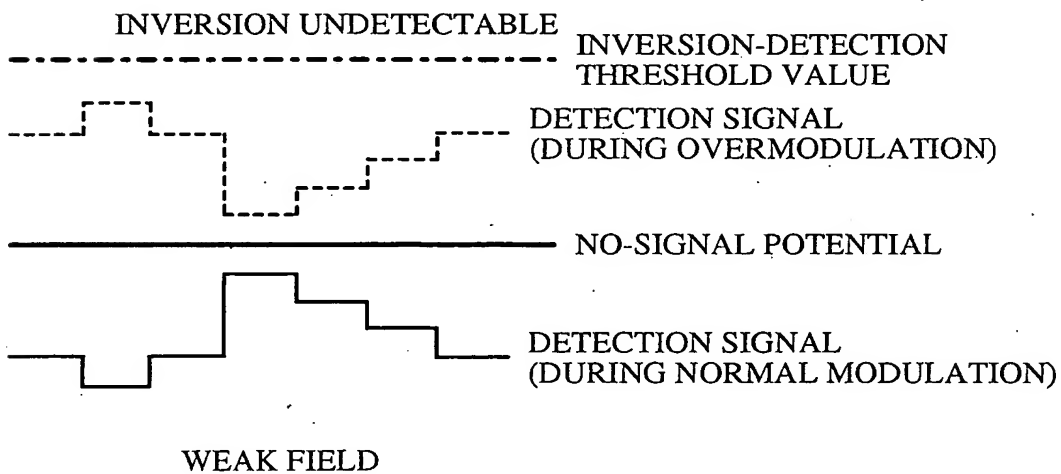
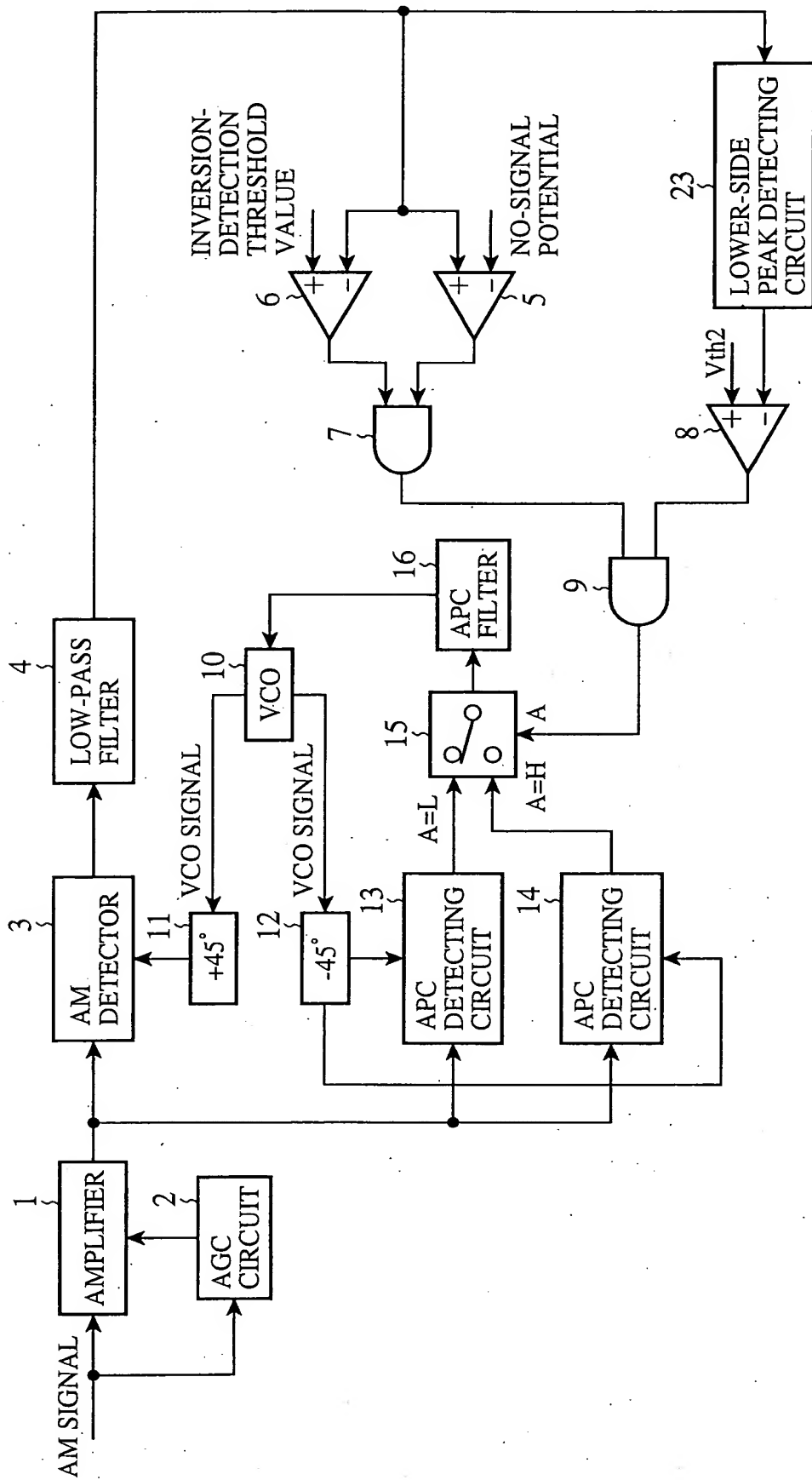


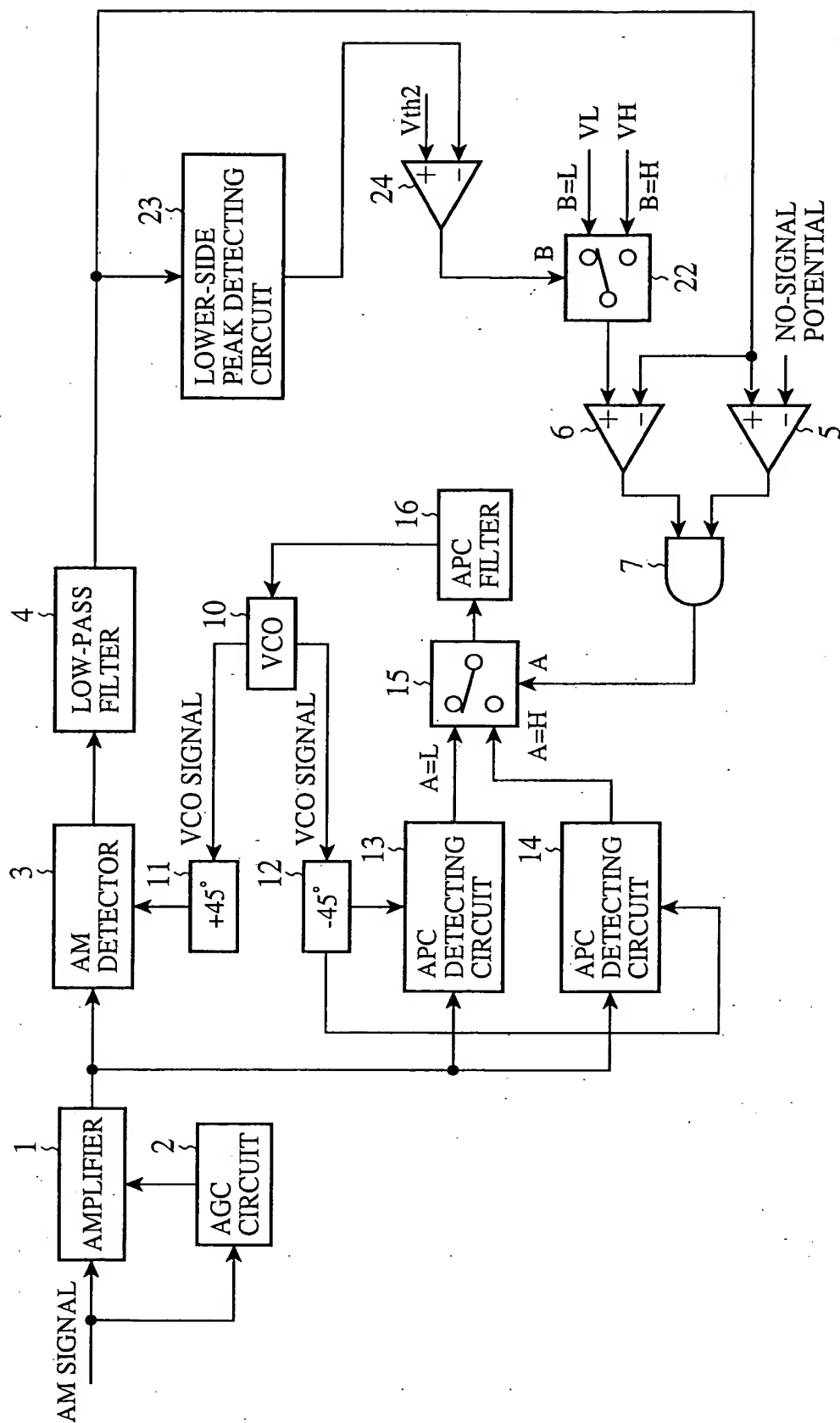
FIG.4



The diagram illustrates a PLL system with AGC and VCO. The input is an AM SIGNAL, which is fed into an AMPLIFIER (1) and an AGC CIRCUIT (2). The AGC CIRCUIT (2) also receives a GAIN CONTROL SIGNAL. The output of the AMPLIFIER (1) is fed into an AM DETECTOR (3). The output of the AM DETECTOR (3) is fed into a LOW-PASS FILTER (4). The output of the LOW-PASS FILTER (4) is fed into a VCO (10). The output of the VCO (10) is fed into a +45° phase shifter (11) and a -45° phase shifter (12). The output of the +45° phase shifter (11) is fed into the AM DETECTOR (3). The output of the -45° phase shifter (12) is fed into an APC DETECTING CIRCUIT (13). The output of the APC DETECTING CIRCUIT (13) is fed into an APC FILTER (16). The output of the APC FILTER (16) is fed into an APC DETECTING CIRCUIT (14). The output of the APC DETECTING CIRCUIT (14) is fed into the AGC CIRCUIT (2). The output of the APC DETECTING CIRCUIT (13) is also fed into a switch (15) with inputs A=L and A=H. The output of the switch (15) is fed into the VCO (10). The output of the VCO (10) is also fed into a switch (22) with inputs B=L and B=H. The output of the switch (22) is fed into a summing junction (6) with inputs VL and VH. The output of the summing junction (6) is fed into a summing junction (5) with inputs NO-SIGNAL and POTENTIAL. The output of the summing junction (5) is fed into a summing junction (21) with inputs Vth1 and -. The output of the summing junction (21) is fed into the VCO (10).

FIG. 6





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FIG.8

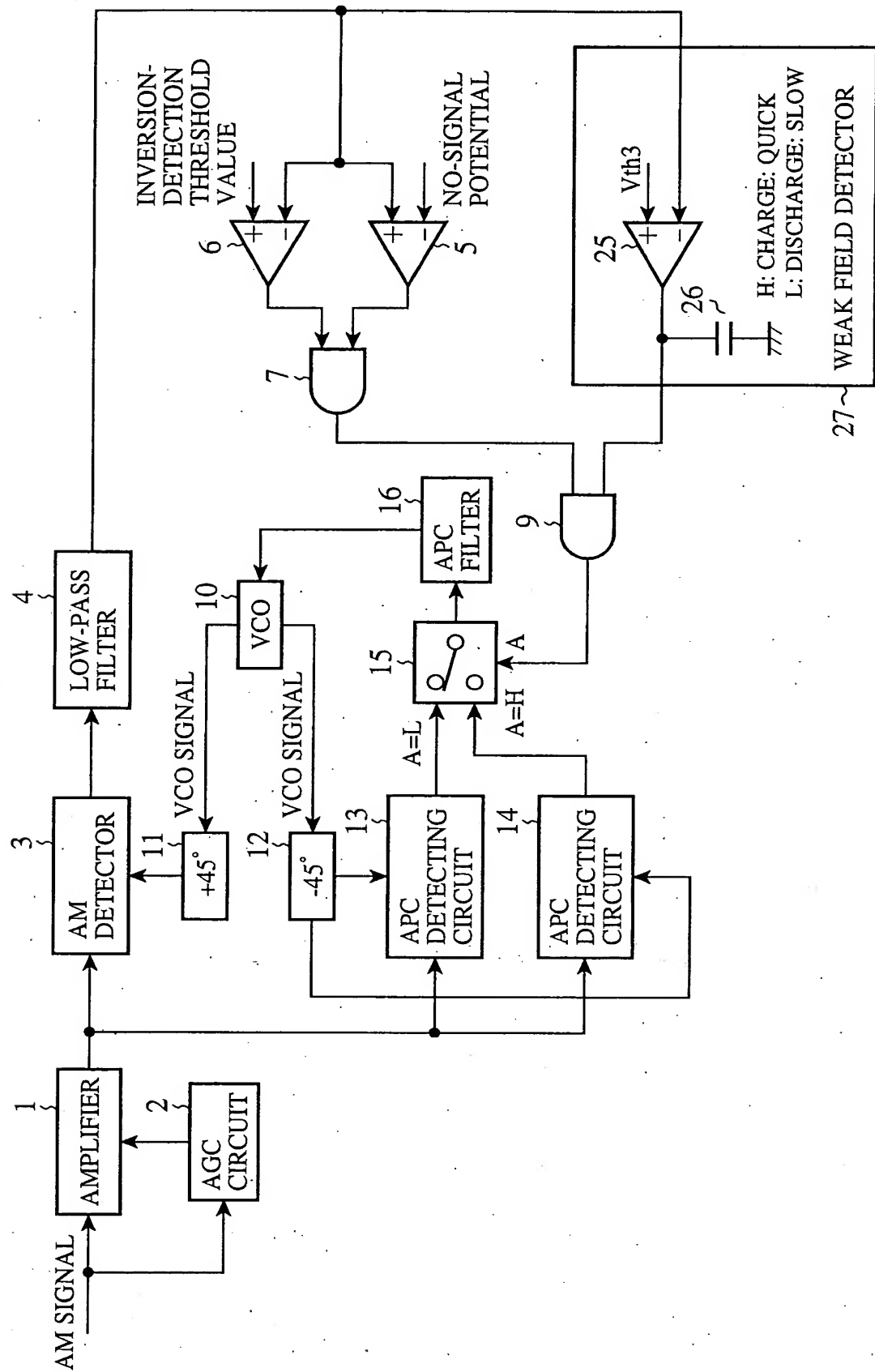


FIG. 9

